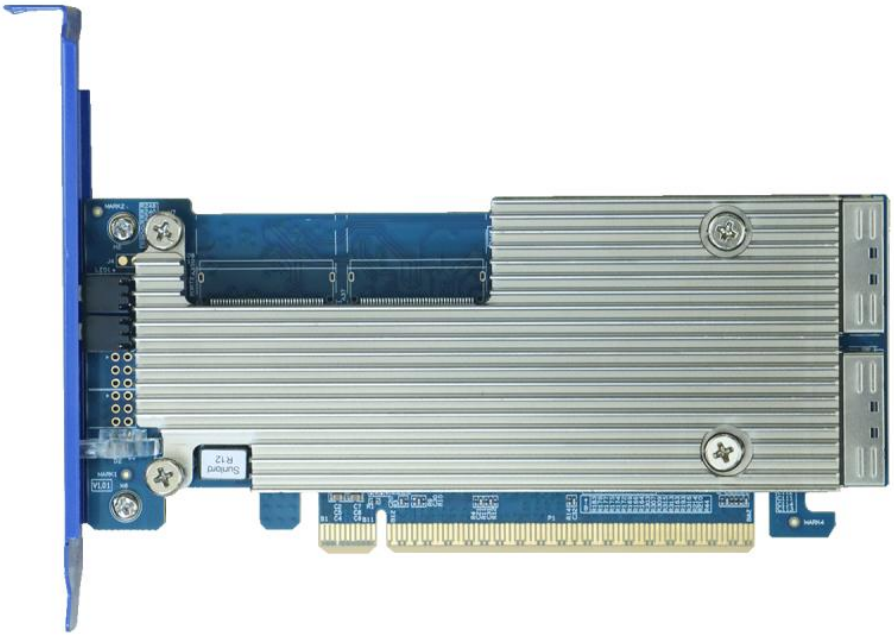
Rocket 1624A (R1624A)

NVMe Switch Adapter User Guide



V1.00 - October 11, 2025

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1. Overview

The R1624A is the latest member of our PCIe Gen5 NVMe Switch Adapter product family.

HighPoint Rocket Series NVMe connectivity adapters address the needs of solution providers and system integrators that cater to vertical marketplaces for high-speed industrial, corporate, and media applications. They were designed for professional applications that demand uncompromised storage performance, scalability, and adaptability in a compact, easy-to-integrate package that is universally compatible with industry-standard x86-64 (Intel/AMD) platforms.

The R1624A's two independent device ports can support U.2/U.3/E3.S NVMe SSDs via versatile cabling solutions.

All major Windows operating systems and current distributions of Linux natively support the R1624A. You won't need to juggle a series of device drivers, install a complex software suite, or master a specialized management interface. Your NVMe SSDs will be automatically recognized and can be prepped and mounted using the operating system's standard tool set.

1.1. Key Features

- Dedicated PCIe 5.0 x16 host interface
- Support data transfer rate 64GB/s
- Provide two internal MCIO (SFF-1016 8x) connectors
- Support four dedicated U.2/U.3/E3.S NVMe devices
- Complies with SFF-9402 standard
- Provide a full-height bracket and a low-profile bracket
- True NVMe Hot-Swap capability
- FRU Inventory support
- Downstream port containment
- Read tracking
- Synthetic hierarchy
- Software Secure Boot
- Hardware Secure Boot
- Out-Of-band Support - BMC Support
- Complies with SFF-TA-1005 specification for Universal Backplane Management (UBM)
- Support VPP Backplane
- Support UBM Backplane
- Support LED Management
- Support all the operating systems with a native NVMe driver

1.1.1. FRU

The *Field Replacement Unit (FRU)* ensures smooth operation and efficient maintenance of complex systems. The unit is designed to house and protect vital product data (VPD).

Information fields within a VPD resource type contain a three-byte header and some data. The three-byte header contains a two-byte keyword and a one-byte length. A keyword is a two-character (ASCII) mnemonic that uniquely identifies the information in the field. The last byte of the header is binary and represents the length value (in bytes) of the following data.

In the event of a hardware failure, the *FRU* can be quickly replaced, returning the device to a fully functional state without requiring extensive diagnostics or data recovery. This reduces downtime and minimizes the possibility of data loss, ensuring that critical operations can continue uninterrupted.

The following table describes the details and descriptions of the VPD.

Table 1: Details and Descriptions of the VPD

Key Word	Details	Descriptions
PN	AIC Part Number	This keyword is an extension to the Device ID (or Subsystem ID) in the Configuration Space header.
EC	Engineering Change Level	The characters are alphanumeric and represent the engineering change level for this add-in card.
MN	Manufacture ID	This keyword is provided as an extension to the Vendor ID (or Subsystem Vendor ID) in the Configuration Space header. This allows vendors to identify an additional level of detail regarding the sourcing of this device.
SN	Serial Number	The characters are alphanumeric and represent the unique add-in card Serial Number.
Vx	Vendor Specific	This is a vendor-specific item, and the characters are alphanumeric. The keyword's second character (x) can be 0 through 9 or A through Z. V0 indicates the Vendor Name V1 indicates the Main Chip

1.1.2. Synthetic Hierarchy

Synthetic Hierarchy is a firmware-driven PCI/PCIe hierarchy management scheme where hardware redirects configuration requests to firmware via TLP redirection. Firmware dynamically constructs host-specific and Arm-side hierarchies by programming address/ID traps for TLP routing, enabling flexible adaptation in multi-host systems without direct hardware enumeration.

1.1.3. Hardware Secure Boot

The secure boot feature permits only authenticated firmware to execute. The switch boots the root of the trusted firmware from the internal boot ROM(IBR)and uses that firmware to authenticate the external firmware stored in the SPI flash and prevent the execution of unauthenticated code.

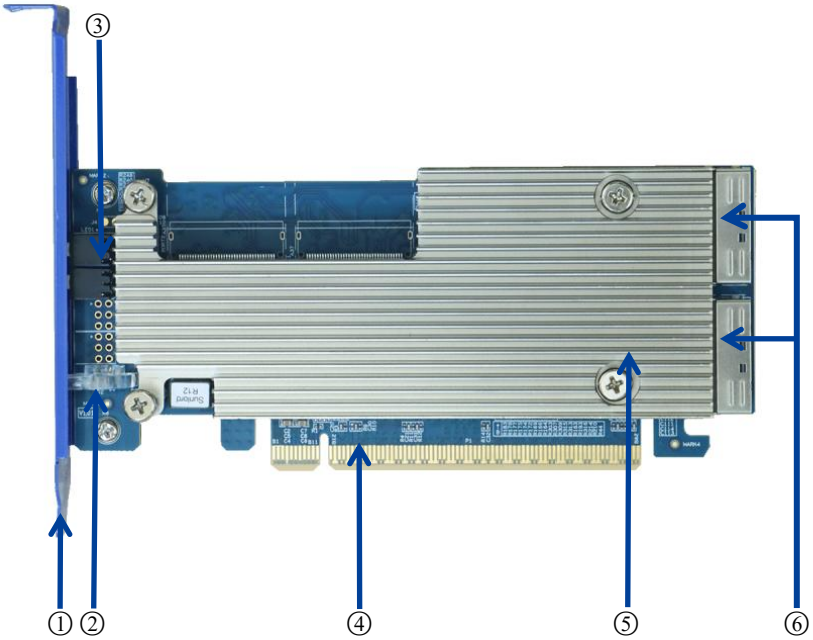
2. R1624A Hardware Description

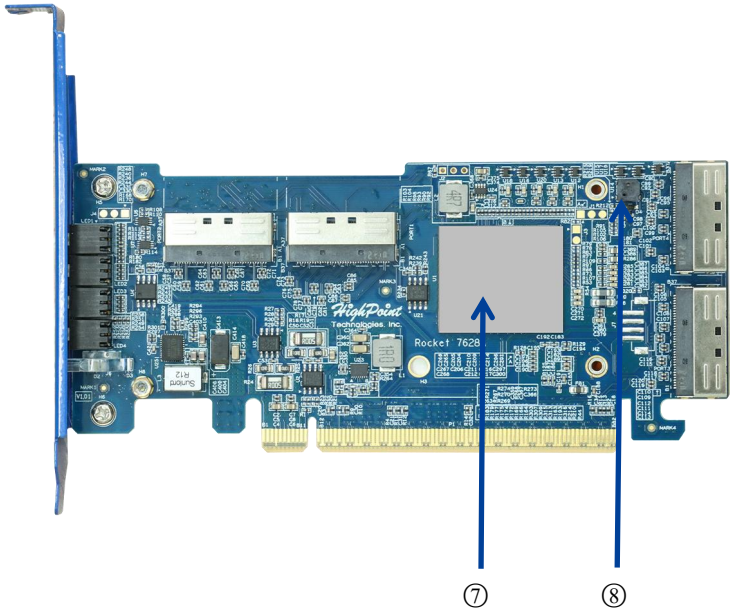
2.1. R1624A Layout

The layout of the R1624A is presented in two parts.

2.1.1. Front View

The following figure shows the key components of the R1624A.





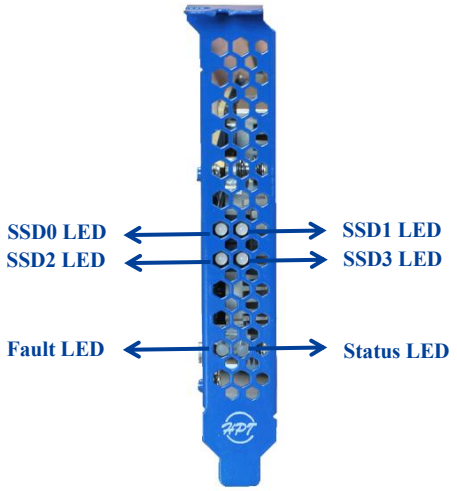
The following table describes the key components of the R1624A.

Table 2: Key component of the R1624A

Number	Type	Description
①	Bracket	Full-height bracket (optional low-profile bracket included). The R1624A is secured to the chassis by a bracket.
②	RGB	Status LED and Fault LED. ● Status LED -- The state of R1624A PCIe bandwidth ● Fault LED -- The state of the Broadcom chipset temperature.
③	LED	Four SSD LED. SSD LED indicates the state of SSD bandwidth.
④	PCIe Host Interface	PCIe 5.0 x16 host interface. The interface between the R1624A and the host system. With the PCIe interface, this connector provides power to the board.
⑤	Cooling System	Passive Heatsink They are used to dissipate heat from electronic components prone to heat generation.
⑥	Storage Interface	Two MCIO (SFF-1016 8x) internal connectors. Connect the R1624A by cable to the storage devices.
⑦	Chip	Broadcom PEX 89048 chip.
⑧	Beeper	Only to be used for field testing.

2.1.2. Diagnostic LED View

The following figure shows the LED Indicators of the R1624A.



The following table describes the SSD LED, Status LED, and Fault LED of the R1624A.

Table 3: LED Indicators of the R1624A

LED	Color	Status	Description
SSD LED		**OFF**	The R1624A is powered off, or the SSD is not detected.
		Solid Green	The SSD is detected.
		Solid Red	The SSD has failed.
Status LED		**OFF**	The R1624A is powered off.
	Notes: The LED blinks blue twice in the first second, then goes out for one second and continues to cycle this process. The following represents the bandwidth status of the R1624A.		
		Interval Flash Blue	PCIe 5.0 x16.
		Interval Flash Green	PCIe 5.0 x8 or PCIe 4.0 x16.
		Interval Flash Yellow	PCIe 5.0 x4, PCIe 4.0 x8, or PCIe 3.0 x16.
		Interval Flash Cyan	PCIe 4.0 x4 or PCIe 3.0 x8.
		Interval Flash White	PCIe 3.0 x4.
		Interval Flash Red	Not appear as above.
Fault LED		**OFF**	The R1624A is powered off.
		Fast Flash Red	The LED blinks red at 4 Hz to indicate that the Broadcom chipset temperature has exceeded the recommended temperature threshold (105℃)

2.2. PCIe Host Interface

The R1624A's PCIe 5.0 host interface provides maximum transmission. Other PCIe host interface features include the following:

- 16-lane PCIe host interface
- Support of x16 link width
- 16-lane aggregate bandwidth of up to 64GB/s

2.3. Storage Interface

The R1624A has two MCIO (SFF-1016 8x) interfaces. Other storage interface features include the following:

- Dedicated PCIe 5.0 x4 per port
- Supports up to four NVMe devices (up to x4 lanes, U.2/U.3/E3.S media)
- Data transfer at 16 GB/s

2.4. Basic Specifications

The following table describes the basic specifications of the R1624A.

Table 4: Basic Specifications of R1624A

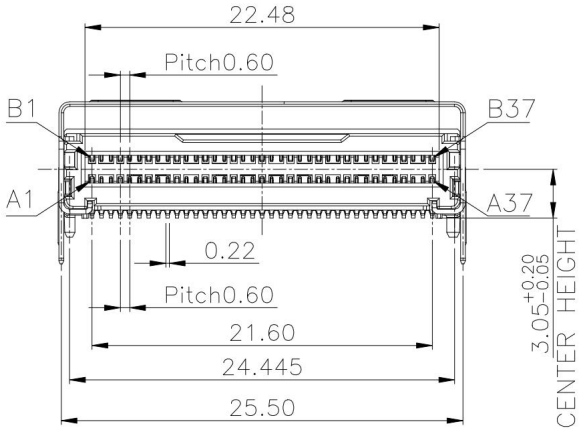
Model		**R1624A**
Form Factor		LP-MD2, Single Width
Weight		180g
Dimension	**Length**	6.10"
	Height	2.72"
Power consumption		● **Idle mode**: 10.84W ● **I/Os mode**: 16.62W Notes: TheI/Os mode power consumption is measured with the four KIOXIA CM7-V series NVMe SSDs. Actual power consumption may differ based on system hardware and configuration.
Power supply		PCIe: 12V(±8%), 3.3V (±8%)
Work temperature		0°C ~ + 55°C
Storage temperature		-20°C ~ +80°C
MTBF (Mean Time Before Failure)		> 5,000,000 hours at 40°C

3. R1624A MCIO Connector

3.1. MCIO Connector Pin Designation

The R1624A has two x8 MCIO connectors, each designated A and B. It follows the SFF-9402 standard for connector sideband signal assignments.

The following figure shows the MCIO connector pin designation.



3.2. MCIO Connetor Pinout

The following table defines the R1624A's MCIO connector pinouts.

Table 5: MCIO Connector Pinouts

Pin	Name	Pin	Name
A1	GND	B1	GND
A2	PERp0	B2	PETp0
A3	PERn0	B3	PETn0
A4	GND	B4	GND
A5	PERp1	B5	PETp1
A6	PERn1	B6	PETn1
A7	GND	B7	GND
A8	BP_TYPEA(VSPA)	B8	2W-CLKA
A9	CWAKEA#,OBFFA(VSPA)	B9	2W-DATAA
A10	Sideband2	B10	Sideband1
A11	REFCLKA+(VSPA+)	B11	PERSTA#(VSPA)
A12	REFCLKA-(VSPA-)	B12	CPRSNTA#(VSPA)

A13	GND	B13	GND
A14	PERp2	B14	PETp2
A15	PERn2	B15	PETn2
A16	GND	B16	GND
A17	PERp3	B17	PETp3
A18	PERn3	B18	PETn3
A19	GND	B19	GND
A20	PERp4	B20	PETp4
A21	PERn4	B21	PETn4
A22	GND	B22	GND
A23	PERp5	B23	PETp5
A24	PERn5	B24	PETn5
A25	GND	B25	GND
A26	BP_TYPEB(VSPB)	B26	2W-CLKB(VSPB)
A27	CWAKEB#,OBFFB(VSPB)	B27	2W-DATAB(VSPB)
A28	Sideband4	B28	Sideband3
A29	REFCLKB+(VSPB+)	B29	PERSTB#(VSPB)
A30	REFCLKB-(VSPB-)	B30	CPRSNTB#(VSPB)
A31	GND	B31	GND
A32	PERp6	B32	PETp6
A33	PERn6	B33	PETn6
A34	GND	B34	GND
A35	PERp7	B35	PETp7
A36	PERn7	B36	PETn7
A37	GND	B37	GND

3.3. Backplane Connector Support

The R1624A supports the industry-standard SFF-TA-1005 Specification for Universal Backplane Management (UBM). UBM provides the following key features:

- Reports the backplane capabilities, including the following:
  - NVMe drive widths
  - Maximum speeds
  - Dual-port support
  - Support for drive power enable and disable (PWDIS)
- Supports cable order independence
  - Disk LED control and slot ID are not dependent on cable order
- Enables disk hot-plug insertion

3.3.1. UBM Backplane

The SFF-TA-1005 (UBM) standard-compliant backplanes are designed to transmit slot numbers to the R1624A automatically. This innovation eliminates the need to manually configure cables between the R1624A and the backplane connector, optimizing cable flexibility.

3.3.1.1. UBM Backplane with x8 Connectors

The following figures show a backplane using x8 connectors with one UBM target per connector. The red lines indicate the I_2C bus connections. For the backplane LEDs to function properly and the disks to be recognized properly, it is imperative that the backplane connects the I_2C connection of the UBM target to the specific x8 MCIO connector. To ascertain which host-facing connector corresponds to a specific slot, please refer to the backplane's documentation.

Note: In order to recognize the disk correctly, please connect all the required cables before use. Prioritize the power supply to the backplane and disks, then to the host, or supply power simultaneously.

Figure 1 UBM Backplane with x8 Connectors (4 Disks)

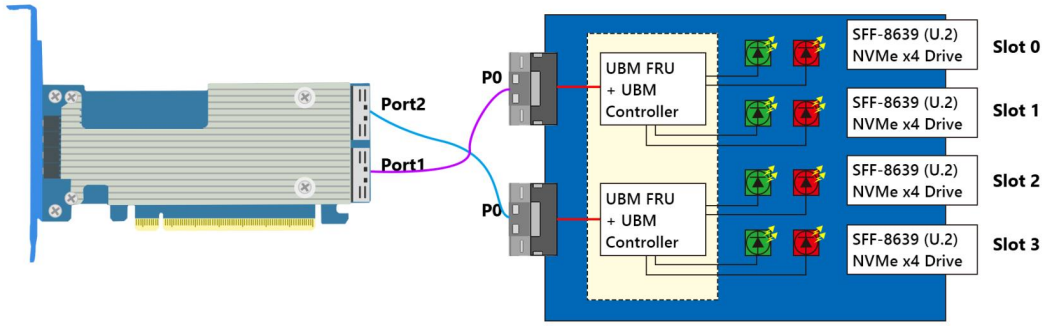
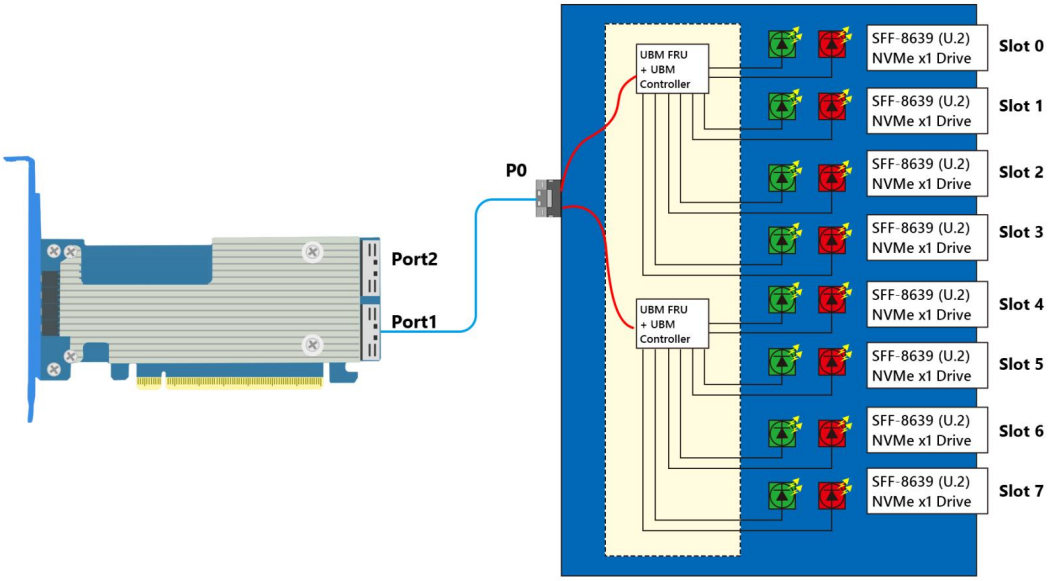


Figure 2 UBM Backplane with x8 Connectors (16 Disks)



Note: For the connection of Port2, please refer to Port1.

3.3.1.2. UBM Backplane with x4 Connectors

The following figures show a backplane using x4 connectors with one UBM target per connector. The red lines indicate the I_2C bus connections. Or the backplane LEDs to function properly and the disks to be recognized properly, it is imperative that the backplane connects the I_2C connection of the UBM target to the specific x4 MCIO connector. To ascertain which host-facing connector corresponds to a specific slot, please refer to the backplane's documentation.

Note: In order to recognize the disk correctly, please connect all the required cables before use.

Prioritize the power supply to the backplane and disks, then to the host, or supply power simultaneously.

Figure 3 UBM Backplane with x4 Connectors (4 Disks)

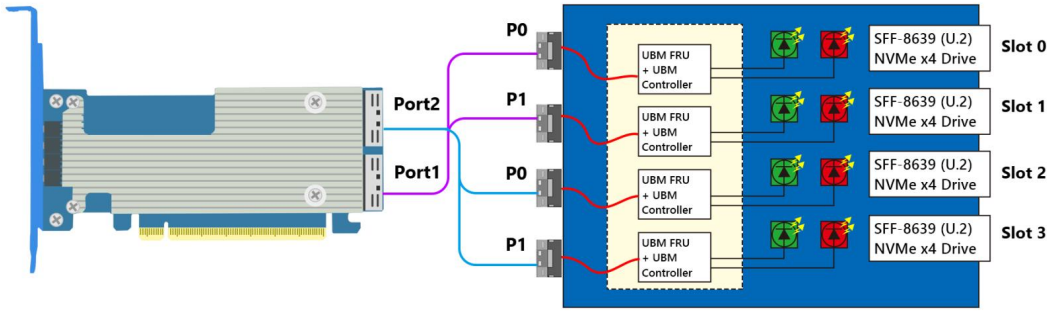
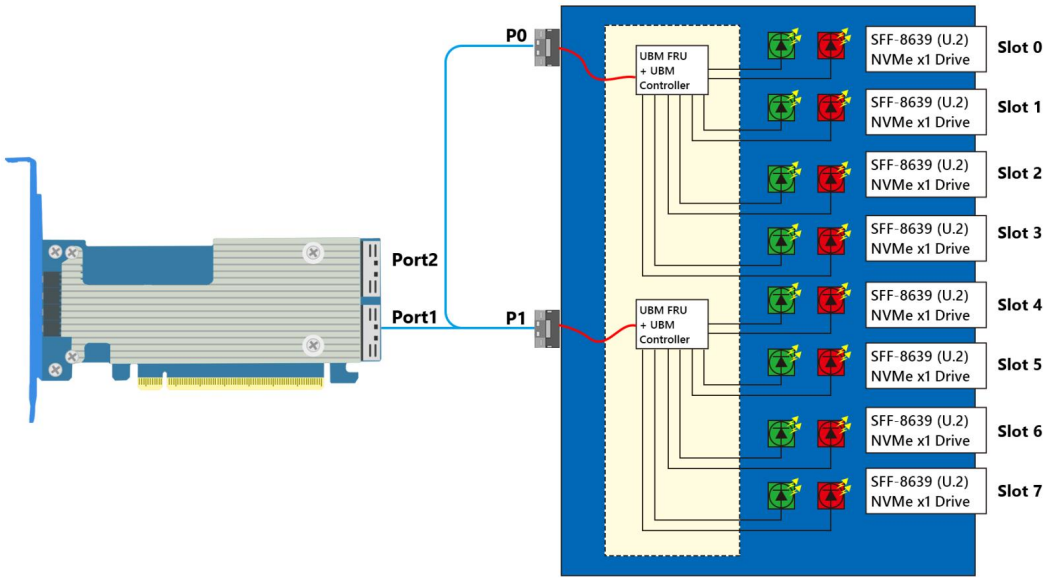


Figure 4 UBM Backplane with x4 Connectors (16 Disks)

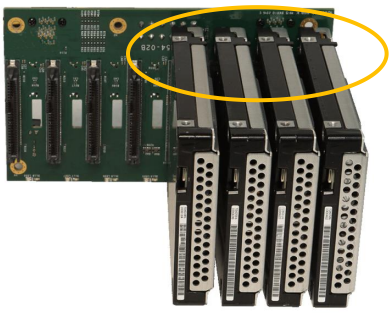


Note: For the connection of Port2 please refer to Port1.

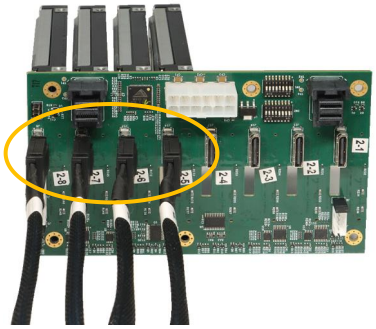
3.3.1.3. UBM Backplane Connection (4 Disks)

The following steps show the connection of the UBM backplane to the R1624A.

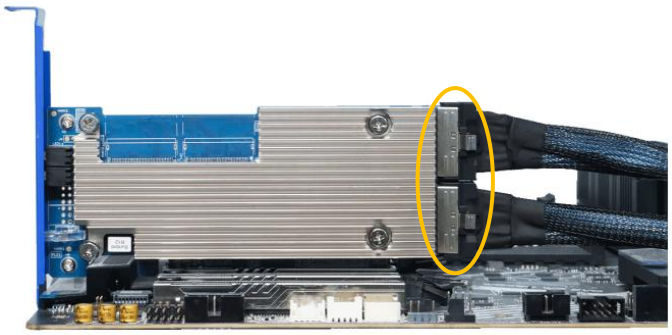
1. Connect the disks to the backplane.



2. Connect the SFF-8611 connectors to the backplane.



3. Connect the MCIO connector to the R1624A.

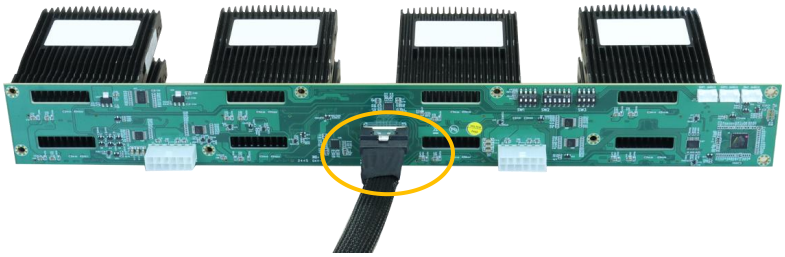


3.3.1.4. UBM Backplane Connection (16 Disks)

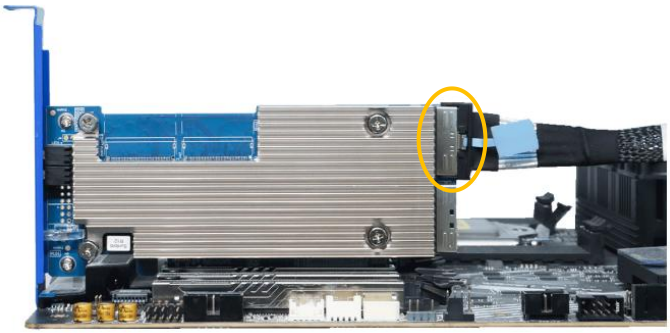
The following steps show the connection of the UBM backplane to the R1624A.

1. Connect the disks to the backplane.

2. Connect the SFF-8654 connector to the backplane.



3. Connect the MCIO connector to the R1624A.



Note: For the connection of Port1, please refer to Port2.

3.3.2. VPP Backplane

The R1624A supports the legacy implementation of Virtual Pin Port (VPP) backplane management. The cables must be connected according to the desired slot enumeration to identify the slots correctly. Connect the MCIO connector of the R1624A to the backplane via the cable.

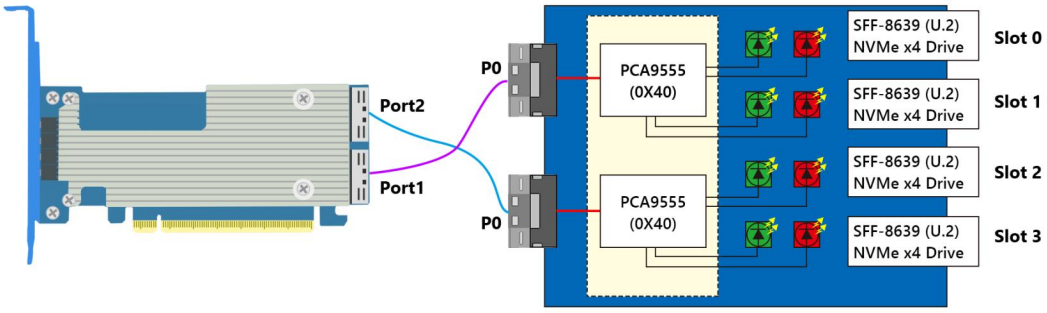
3.3.2.1. Backplane with x8 Connectors and VPP

The figures below illustrate the anticipated connections to a backplane, utilizing x8 MCIO connectors from the Adapter to NVMe disks, with VPP over I_2C employed for managing the backplane. The red line highlights the I_2C bus connection. Or the backplane LEDs to function properly and the disks to be recognized properly, it is imperative that the backplane connects the I_2C connection of the VPP target to the specific x8 MCIO connector. To ascertain which host-facing connector corresponds to a specific slot, please refer to the backplane's documentation.

Note: In order to recognize the disk correctly, please connect all the required cables before use.

Prioritize the power supply to the backplane and disks, then to the host, or supply power simultaneously.

Figure 5 Backplane with x8 Connectors and VPP (4 Disks)



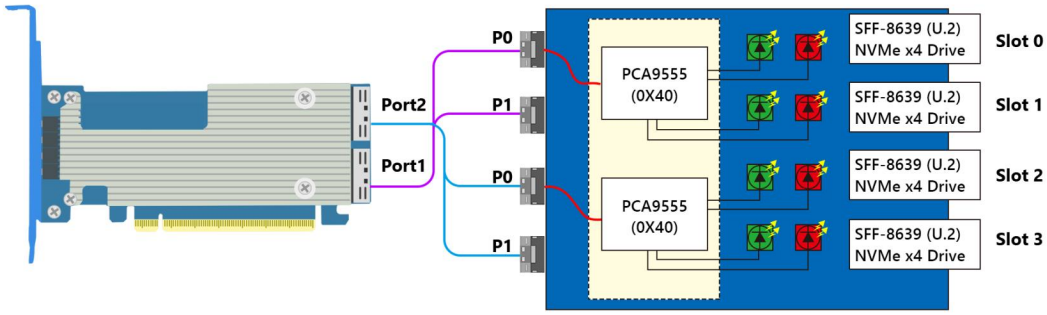
3.3.2.2. Backplane with x4 Connectors and VPP

The figure below illustrates the anticipated connections to a backplane, utilizing x4 MCIO connectors from the Adapter to NVMe disks, with VPP over I_2C employed for managing the backplane. The red line highlights the I_2C bus connection. or the backplane LEDs to function properly and the disks to be recognized properly, when using HighPoint supplied cables, connect the P0 labeled leg of the cable to the PCA9555 target. To ascertain which host-facing connector corresponds to a specific slot, please refer to the backplane's documentation.

Note: In order to recognize the disk correctly, please connect all the required cables before use.

Prioritize the power supply to the backplane and disks, then to the host, or supply power simultaneously.

Figure 6 Backplane with x4 Connectors and VPP (4 Disks)



4. Cable Accessories

A wide selection of flexible cabling options is available for the R1624A, which enable the NVMe Switch Adapter to mix configurations of U.2/U.3/E3.S NVMe SSDs via SFF-8639, SFF-8654, SFF-TA-1002, and MCIO connectors.

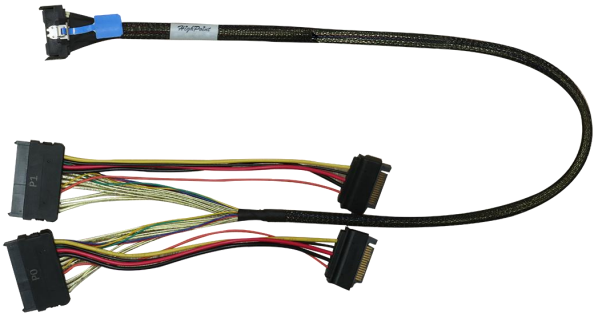
The following sections indicate the cable pinout and connection diagram for supported cable accessories.

4.1. CIO8-8639-110

MCIO (x8) Host to SFF-8639 Device cable with a 15-pin SATA power connector. Each cable supports two U.2 NVMe SSDs. Length 1M.

4.1.1. Cable Diagram

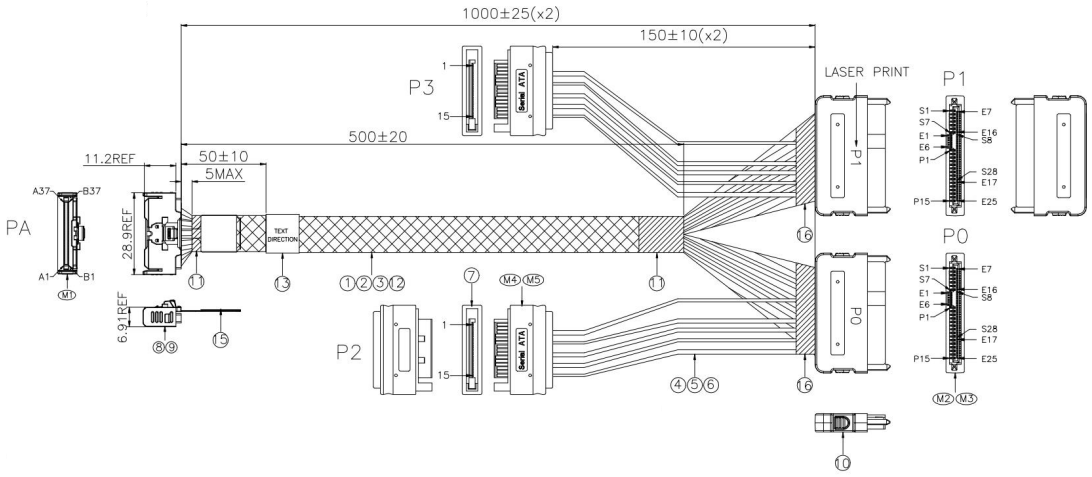
MCIO

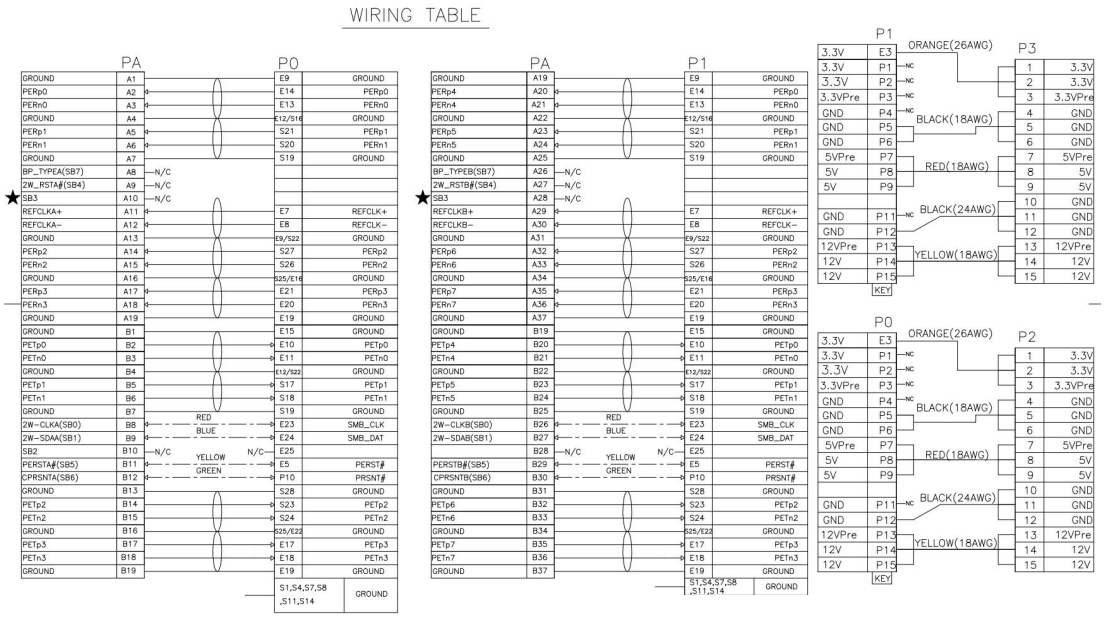


SFF-8639

4.1.2. Cable Drawings and Pinouts

The following figure shows the pinout for the HighPoint CIO8-8639-110 cable, one x8 MCIO to two x4 SFF-8639 connection.

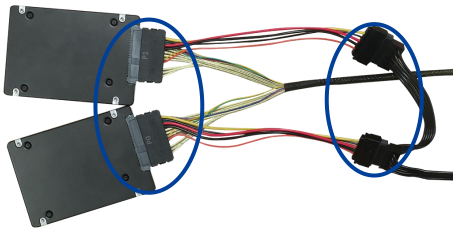




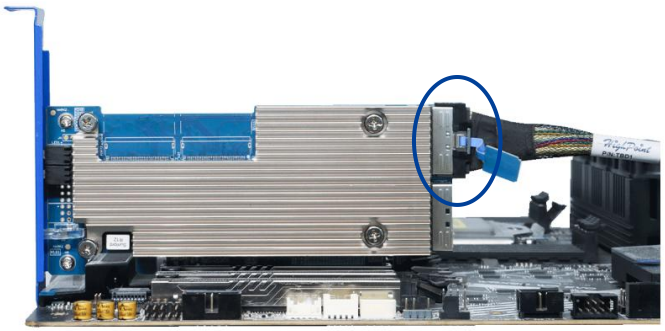
4.1.3. Cable Connection

The following steps show the connection of a U.2 SSD to the R1624A using the CIO8-8639-110 cable.

1. Connect the SFF-8639 connector of the CIO8-8639-110 cable to the NVMe SSD, and connect the 15-pin SATA power connector to the power supply.



2. Connect the SFF-8639 connector of the CIO8-8639-110 cable to the R1624A.



4.2. CIO8-CIO8-110

MCIO Host to MCIO Device cable. Each cable can host up to two NVMe SSDs. Length 1M.

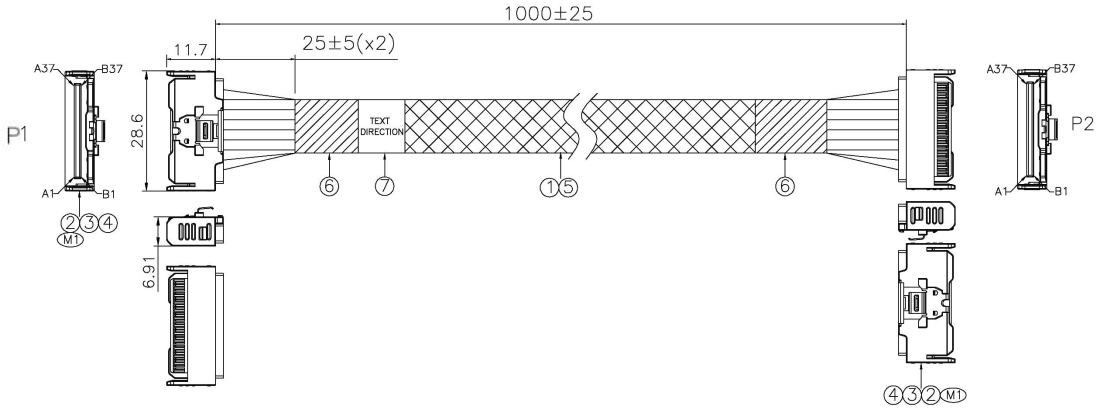
4.2.1. Cable Diagram

MCIO

MCIO

4.2.2. Cable Drawings and Pinouts

The following figure shows the pinout for the HighPoint CIO8-CIO8-110 cable, one x8 MCIO to one x8 MCIO connection.



WIRING TABLE

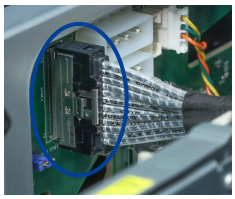
P1		P2	
GROUND	B37	A37	GROUND
TX7−	B36	A36	RX7−
TX7+	B35	A35	RX7+
GROUND	B34	A34	GROUND
TX6−	B33	A33	RX6−
TX6+	B32	A32	RX6+
GROUND	B31	A31	GROUND
SB4−	B30	A30	SB8−
SB4+	B29	A29	SB8+
GROUND	B28	A28	GROUND
SB3−	B27	A27	SB7−
SB3+	B26	A26	SB7+
GROUND	B25	A25	GROUND
TX5−	B24	A24	RX5−
TX5+	B23	A23	RX5+
GROUND	B22	A22	GROUND
TX4−	B21	A21	RX4−
TX4+	B20	A20	RX4+
GROUND	B19	A19	GROUND
TX3−	B18	A18	RX3−
TX3+	B17	A17	RX3+
GROUND	B16	A16	GROUND
TX2−	B15	A15	RX2−
TX2+	B14	A14	RX2+
GROUND	B13	A13	GROUND
SB2−	B12	A12	SB6−
SB2+	B11	A11	SB6+
GROUND	B10	A10	GROUND
SB1−	B9	A9	SB5−
SB1+	B8	A8	SB5+
GROUND	B7	A7	GROUND
TX1−	B6	A6	RX1−
TX1+	B5	A5	RX1+
GROUND	B4	A4	GROUND
TX0−	B3	A3	RX0−
TX0+	B2	A2	RX0+
GROUND	B1	A1	GROUND

P1		P2	
GROUND	A37	B37	GROUND
RX7−	A36	B36	TX7−
RX7+	A35	B35	TX7+
GROUND	A34	B34	GROUND
RX6−	A33	B33	TX6−
RX6+	A32	B32	TX6+
GROUND	A31	B31	GROUND
SB8−	A30	B30	SB4−
SB8+	A29	B29	SB4+
GROUND	A28	B28	GROUND
SB7−	A27	B27	SB3−
SB7+	A26	B26	SB3+
GROUND	A25	B25	GROUND
RX5−	A24	B24	TX5−
RX5+	A23	B23	TX5+
GROUND	A22	B22	GROUND
RX4−	A21	B21	TX4−
RX4+	A20	B20	TX4+
GROUND	A19	B19	GROUND
RX3−	A18	B18	TX3−
RX3+	A17	B17	TX3+
GROUND	A16	B16	GROUND
RX2−	A15	B15	TX2−
RX2+	A14	B14	TX2+
GROUND	A13	B13	GROUND
SB6−	A12	B12	SB2−
SB6+	A11	B11	SB2+
GROUND	A10	B10	GROUND
SB5−	A9	B9	SB1−
SB5+	A8	B8	SB1+
GROUND	A7	B7	GROUND
RX1−	A6	B6	TX1−
RX1+	A5	B5	TX1+
GROUND	A4	B4	GROUND
RX0−	A3	B3	TX0−
RX0+	A2	B2	TX0+
GROUND	A1	B1	GROUND

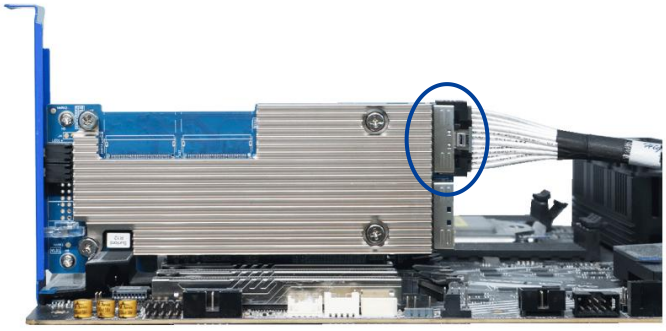
4.2.3. Cable Connection

The following steps show the connection of the backplane to the R1624A using the CIO8-CIO8-110 cable.

1. Connect the MCIO connector of the CIO8-CIO8-110 cable to the backplane.



2. Connect the other MCIO connector of the CIO8-CIO8-110 cable to the R1624A.

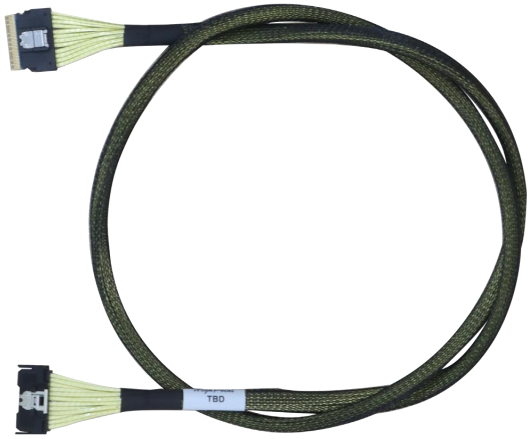


4.3. 8654-CIO8-110

MCIO Host to SFF-8654 Device cable. Each cable can host up to two NVMe SSDs. Length: 1M.

4.3.1. Cable Diagram

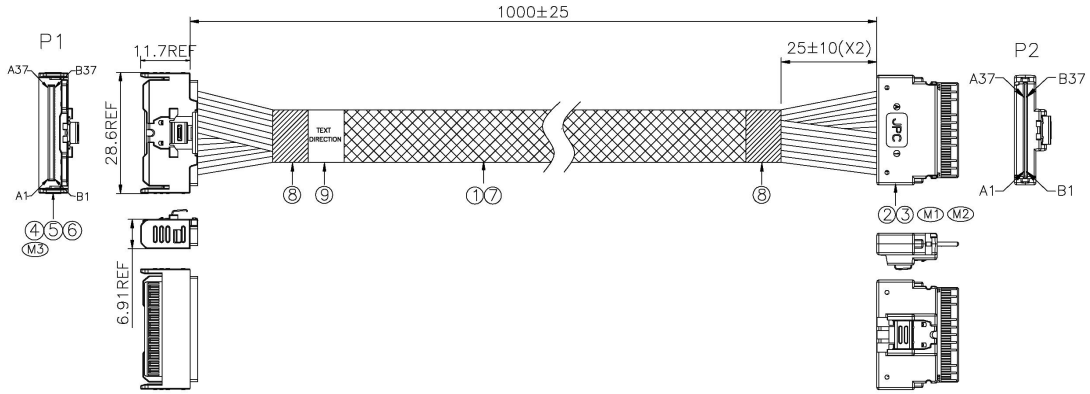
SFF-8654



MCIO

4.3.2. Cable Drawings and Pinouts

The following figure shows the HighPoint 8654- CIO8-110 cable pinout, one x8 MCIO to one x8 SFF-8654 connection.



WIRING TABLE

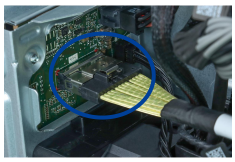
P1			P2		
GROUND	B37	B37	A37	A37	GROUND
TX7−	B36	B36	A36	A36	RX7−
TX7+	B35	B35	A35	A35	RX7+
GROUND	B34	B34	A34	A34	GROUND
TX6−	B33	B33	A33	A33	RX6−
TX6+	B32	B32	A32	A32	RX6+
GROUND	B31	B31	A31	A31	GROUND
SIDEBAND	B30	B30	A30	A30	SIDEBAND
SIDEBAND	B29	B29	A29	A29	SIDEBAND
GROUND	B28	B28	A28	A28	GROUND
SIDEBAND	B27	B27	A27	A27	SIDEBAND
SIDEBAND	B26	B26	A26	A26	SIDEBAND
GROUND	B25	B25	A25	A25	GROUND
TX5−	B24	B24	A24	A24	RX5−
TX5+	B23	B23	A23	A23	RX5+
GROUND	B22	B22	A22	A22	GROUND
TX4−	B21	B21	A21	A21	RX4−
TX4+	B20	B20	A20	A20	RX4+
GROUND	B19	B19	A19	A19	GROUND
TX3−	B18	B18	A18	A18	RX3−
TX3+	B17	B17	A17	A17	RX3+
GROUND	B16	B16	A16	A16	GROUND
TX2−	B15	B15	A15	A15	RX2−
TX2+	B14	B14	A14	A14	RX2+
GROUND	B13	B13	A13	A13	GROUND
SIDEBAND	B12	B12	A12	A12	SIDEBAND
SIDEBAND	B11	B11	A11	A11	SIDEBAND
GROUND	B10	B10	A10	A10	GROUND
SIDEBAND	B9	B9	A9	A9	SIDEBAND
SIDEBAND	B8	B8	A8	A8	SIDEBAND
GROUND	B7	B7	A7	A7	GROUND
TX1−	B6	B6	A6	A6	RX1−
TX1+	B5	B5	A5	A5	RX1+
GROUND	B4	B4	A4	A4	GROUND
TX0−	B3	B3	A3	A3	RX0−
TX0+	B2	B2	A2	A2	RX0+
GROUND	B1	B1	A1	A1	GROUND

P1			P2		
GROUND	A37	A37	B37	B37	GROUND
RX7−	A36	A36	B36	B36	TX7−
RX7+	A35	A35	B35	B35	TX7+
GROUND	A34	A34	B34	B34	GROUND
RX6−	A33	A33	B33	B33	TX6−
RX6+	A32	A32	B32	B32	TX6+
GROUND	A31	A31	B31	B31	GROUND
SIDEBAND	A30	A30	B30	B30	SIDEBAND
SIDEBAND	A29	A29	B29	B29	SIDEBAND
GROUND	A28	A28	B28	B28	GROUND
SIDEBAND	A27	A27	B27	B27	SIDEBAND
SIDEBAND	A26	A26	B26	B26	SIDEBAND
GROUND	A25	A25	B25	B25	GROUND
RX5−	A24	A24	B24	B24	TX5−
RX5+	A23	A23	B23	B23	TX5+
GROUND	A22	A22	B22	B22	GROUND
RX4−	A21	A21	B21	B21	TX4−
RX4+	A20	A20	B20	B20	TX4+
GROUND	A19	A19	B19	B19	GROUND
RX3−	A18	A18	B18	B18	TX3−
RX3+	A17	A17	B17	B17	TX3+
GROUND	A16	A16	B16	B16	GROUND
RX2−	A15	A15	B15	B15	TX2−
RX2+	A14	A14	B14	B14	TX2+
GROUND	A13	A13	B13	B13	GROUND
SIDEBAND	A12	A12	B12	B12	SIDEBAND
SIDEBAND	A11	A11	B11	B11	SIDEBAND
GROUND	A10	A10	B10	B10	GROUND
SIDEBAND	A9	A9	B9	B9	SIDEBAND
SIDEBAND	A8	A8	B8	B8	SIDEBAND
GROUND	A7	A7	B7	B7	GROUND
RX1−	A6	A6	B6	B6	TX1−
RX1+	A5	A5	B5	B5	TX1+
GROUND	A4	A4	B4	B4	GROUND
RX0−	A3	A3	B3	B3	TX0−
RX0+	A2	A2	B2	B2	TX0+
GROUND	A1	A1	B1	B1	GROUND

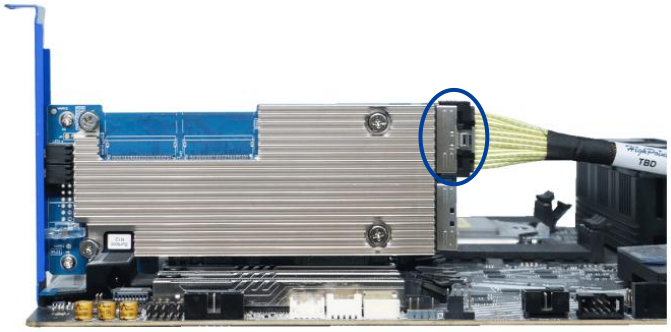
4.3.3. Cable Connection

The following steps show the connection of the backplane to the R1624A using the 8654- CIO8-110 cable.

4. Connect the SFF-8654 connector of the 8654-CIO8-110 cable to the backplane.



5. Connect the MCIO connector of the 8654-CIO8-110 cable to the R1624A.



4.4. CIO8-1002-110

MCIO Host to SFF-TA-1002 Device cable. Each cable can host up to two NVMe SSDs. Length 1M.

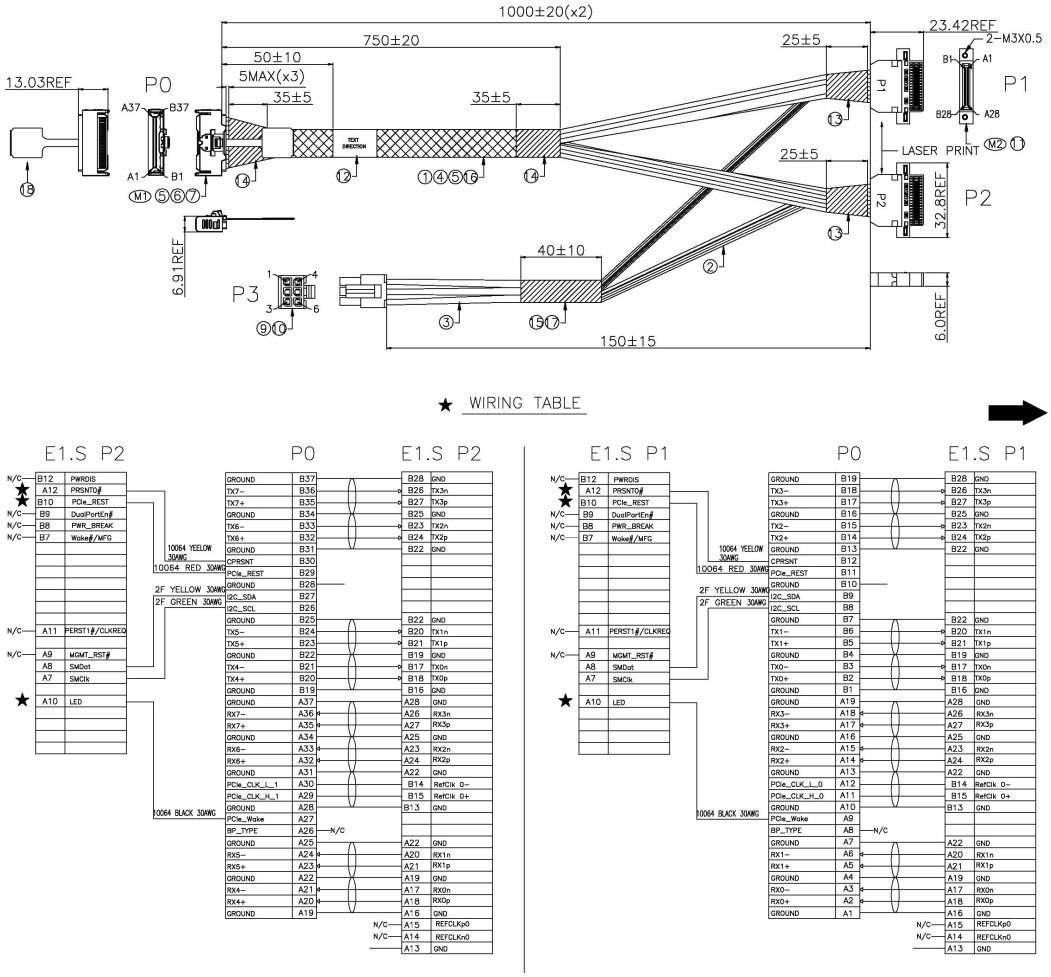
4.4.1. Cable Diagram

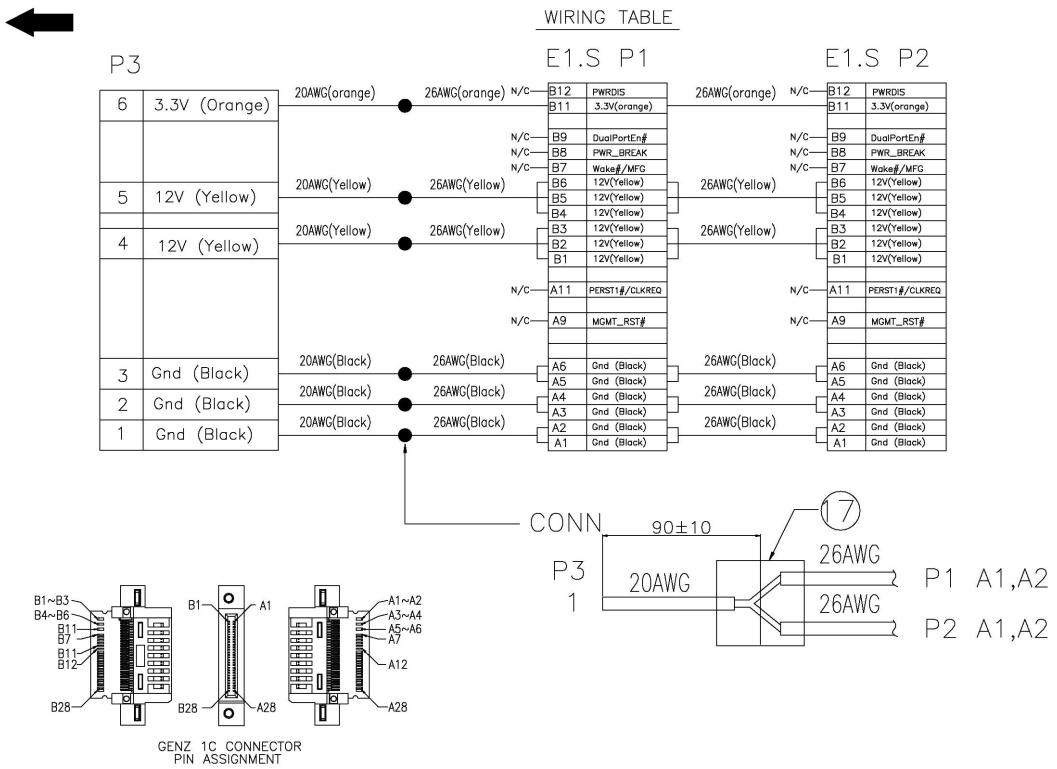
SFF-TA-1002

MCIO

4.4.2. Cable Drawings and Pinouts

The following figure shows the pinout for the HighPoint CIO8-1002-110 cable, one x8 MCIO to two x4 SFF-TA-1002 connection.

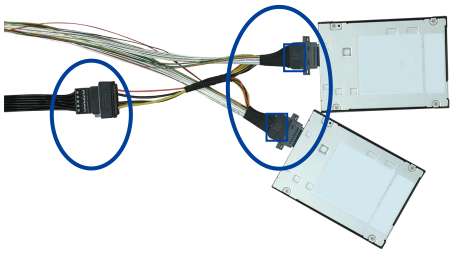




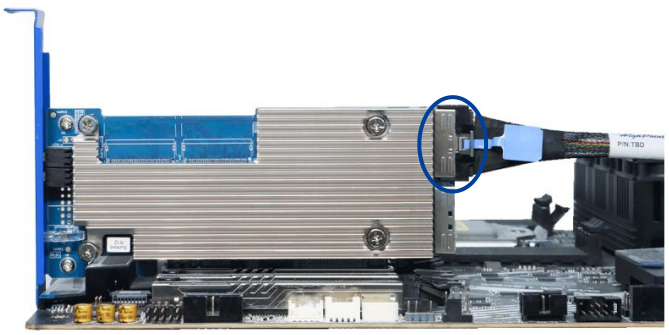
4.4.3. Cable Connection

The following steps show the connection of an NVMe SSD to the R1624A using the CIO8-1002-110 cable.

1. Connect the P1/P2 side of the SFF-TA-1002 connector to the front of the NVMe SSD, and connect the 15-pin SATA power connector to the power supply.



2. Connect the MCIO connector of the CIO8-1002-110 cable to the R1624A.



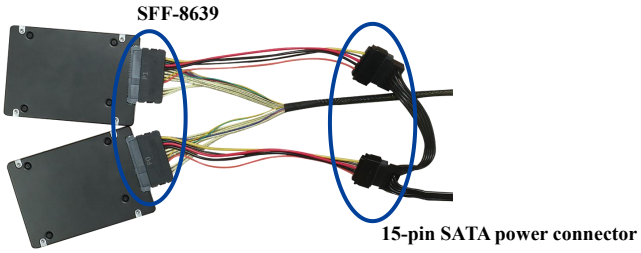
5. R1624A Installation Instructions

The R1624A provides two MCIO connectors. These connectors accept a variety of HighPoint Certified Cable Accessories (see the Accessories section towards the end of this guide for more information). The following steps explain how to connect U.2 NVMe SSDs directly to the R1624A using HighPoint CIO8-8639-110 cable.

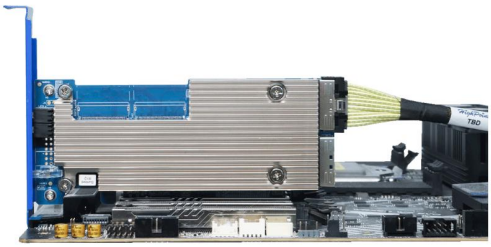
1. Use a wired ESD wrist strap that is properly grounded.
2. Unpack and remove the R1624A and check it for damage. If it appears damaged, please get in touch with HighPoint Technical Support.
3. Shut down the system and disconnect the AC power cord.
4. Align the R1624A to one of the motherboard's available PCIe slots. Press down gently but firmly to seat the R1624A correctly in the slot.

Note: Replace the full-height bracket on the R1624A with the optional low-profile bracket if required by your system.

5. Connect the SFF-8639 connector of the CIO8-8639-110 cable to the NVMe SSD, and connect the 15-pin SATA power connector to the power supply.



6. Connect the MCIO connector of the CIO8-8639-110 cable to the R1624A.



7. Connect the remaining NVMe SSDs to the R1624A as described above.
8. Turn on the power to the system.

Note: Please ensure the cables are securely connected to the R1624A's device ports and the NVMe SSDs or backplanes. Loose connections can lead to various problems, including instability, slower-than-expected performance, and dropped disks.

6. Revision History

6.1. Version 1.00, October 11, 2025

Initial version.